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EXAMINER	
BEDNASH, JOSEPH A	

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2461	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,167	KIM ET AL.	
	Examiner	Art Unit	
	Joey Bednash	2461	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to amendments filed 29 June 2010. Claims 1-12 are pending in the application. Claims 1 and 4-12 are amended. Claim 13 has been cancelled.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 includes the limitation of "a channel decoder for...analyzing modulation methods for each sub-channels..." Claim 1 is directed towards an apparatus and the claim is written in a manner of a means clause (i.e. channel decoder) for performing a specified function (i.e. analyzing modulation methods for each sub-channels). The specification does not provide a description of the structure used to perform the function of "analyzing modulation methods for each sub-channels" therefore it is impossible to determine the equivalents of the element, as required by 35 U.S.C. § 112, sixth paragraph.

Claim Rejections - 35 USC § 103

3. Claims 1 and 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Uesugi et al. (US 2002/0114379 A1), hereinafter "Uesugi".

Regarding claim 1, AAPA discloses a demodulation apparatus for receiving signals by an adaptive modulation and coding method, and demodulating the signals, in an OFDMA based packet communication system, comprising:

a QAM demapper for performing a QAM (Quadrature Amplitude Modulation) demapping process on the received signals **(Fig. 2, QAM Demapper 25)**;

a slot buffer for storing the data outputted from the QAM demapper for each slot **(Fig. 2, Slot Buffers 26; Para [10])**; and

a channel decoder **(Fig. 2, Channel Decoder 27)** for decoding the data stored in the slot buffer **(Para [10])**, for analyzing modulation methods for each sub-channels and transferring the analyzed modulation methods to the QAM demapper **(Para [11], [13])**, and for reading valid data from the data stored in the slot buffer, based on the analyzed modulation methods for each of the sub-channels and demodulating the valid data, and outputting the demodulated data **(Para [10])**.

AAPA does not disclose demapping by a modulation method using a maximum modulation ratio, and outputting data, until modulation methods for each of the sub-channels are analyzed.

Uesugi discloses demapping (i.e. demodulating) a received signal using the largest modulation level map **(Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern; Figs. 5 and 6, Para [0068]-[0074] teaches demapping 16QAM with a 64QAM demodulation pattern; Figs. 7 and 8, Para [0076]-[0080] teaches demapping QPSK with a 64QAM demodulation pattern)**. Uesugi teaches that by demapping (i.e. demodulating)

received QPSK and 16QAM signals using the 64QAM demodulation pattern (i.e. map) without any knowledge of the modulation scheme applied at the transmitter it is possible to decrease data delay **(Para [0095])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to demap (i.e. demodulate) signals using the maximum modulation ratio until the modulation methods for each sub-channels are analyzed because the teaching lies in Uesugi that this approach can decrease data delays.

Regarding claim 4, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the slot buffer comprises:

a first slot buffer for storing data outputted from the QAM demapper until the modulation methods for each of the sub-channels of the received signals are analyzed by the channel decoder **(AAPA: Fig. 2, Slot Buffers 26, it would be obvious that the symbols demapped as taught by Uesugi could be stored in the Slot buffer of Fig. 2)**; and

a second slot buffer for storing data outputted from the QAM demapper, once the modulation methods for each of the sub-channels of the received signals are analyzed by the channel decoder **(AAPA: Fig. 2, Slot Buffers 26, (Fig. 2, Slot Buffers 26; Para [10], Para [11], Para [13])**.

Regarding claim 5, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 4. It would have been merely a matter of obvious engineering design choice with respect to in which slot

buffer illustrated in Fig. 2 of AAPA the demapped data is stored. Storing data demapped by the methods taught by Uesugi in one slot buffer and the data demapped by the conventional methods as taught by AAPA in a different slot buffer would not produce a new and unexpected result.

Regarding claim 6, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the channel decoder reads the MAP information in the former part of a frame among the symbol data stored in the slot buffer, and analyzes the modulation methods for each of the sub-channels **(AAPA, Figs. 1-3, Para [10]-[11]; The Channel decoder 27 decodes data that passes through the slot buffers, and the MAP info is in the former part of the frame.)**.

Regarding claim 7, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the QAM demapper performs a demapping process on the received signals by the modulation methods for each of the sub-channels, and stores the output data in the slot buffer, once the modulation methods for each of the sub-channels are analyzed by the channel decoder **(AAPA, Para [10], [11], [13])**.

Regarding claim 8, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case data are demodulated by the modulation method using the maximum modulation ratio, a constellation for part of the data is identical with a constellation for the data demodulated by the modulation methods for each sub-channels **(Uesugi: Para**

[0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern).

Regarding claim 9, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 8, wherein the demodulation apparatus further comprises:

an FFT (Fast Fourier Transform) unit for performing FFT on the received signals and outputting the signals **(AAPA; Fig. 2, FFT unit 21; Para [10])**;

a re-ordering buffer for re-ordering the signals outputted from the unit and storing the signals **(AAPA; Fig. 2, Reordering Buffers 22; Para [10])**;

an equalizer for estimating channels using the signals stored in the re-ordering buffer and performing equalization of the signals, and outputting the signals to the QAM demapper **(AAPA; Fig. 2, Equalizer 23; Para [10])**.

Regarding claim 10, AAPA in view of Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case the modulation method using the maximum modulation ratio is 64QAM, and a data unit for storing in the slot buffer is 6 bits of data **(Uesugi: Fig. 3)**; the valid data by the 16 QAM modulation method are former 4 bits of data from among the 6 bits of data **(Uesugi: Fig. 5, Para [0074])**.

Regarding claim 11, Uesugi teaches the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein in the case the modulation method using the maximum modulation ratio is 64 QAM, and a data unit for storing in

the slot buffer is 6 bits of data **(Uesugi: Fig. 3)**, the valid data by the QPSK modulation method are 2 bits of data in front of the 6 bits of data **(Uesugi: Fig. 5, Para [0080])**.

Regarding claim 12, AAPA discloses a demodulation method for receiving signals by an adaptive modulation and coding method and demodulating the signals, in an OFDMA based packet communication system, comprising stages of:

a) performing a demapping process on the received signals by a modulation method and storing the signals **(Fig. 2, QAM Demapper 25, Slot Buffer 26, Para [10])**;

b) decoding the demapped and stored signals the and analyzing the modulation methods for each of sub-channels **(Fig. 2, Channel Decoder 27, Para [11])**; and

c) performing a demapping process on the received signals by the analyzed modulation methods for each sub-channels and demodulating the signals **(Para [13])**,

wherein the signals are stored in step a) until the modulation methods for each of the sub-channels are analyzed **(Para [11])**; only valid data from among the signals are read by the modulation methods for each of the sub-channels analyzed in step b); and the valid data are demodulated **(Para [10])**.

AAPA does not teach using a maximum modulation ratio for the demapping process.

Uesugi discloses demapping (i.e. demodulating) a received signal using the largest modulation level map **(Para [0094]; Figs. 3 and 4, Para [0060]-[0067] teaches demapping 64QAM with a 64QAM demodulation pattern; Figs. 5 and 6, Para [0068]-[0074] teaches demapping 16QAM with a 64QAM demodulation pattern; Figs. 7 and 8, Para [0076]-[0080] teaches demapping QPSK with a 64QAM**

demodulation pattern). Uesugi teaches that by demapping (i.e. demodulating) received QPSK and 16QAM signals using the 64QAM demodulation pattern (i.e. map) without any knowledge of the modulation scheme applied at the transmitter it is possible to decrease data delay **(Para [0095])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to demap (i.e. demodulate) signals using the maximum modulation ratio until the modulation methods for each sub-channels are analyzed because the teaching lies in Uesugi that this approach can decrease data delays.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Uesugi, further in view of Matsumoto et al. (US 2002/0136207 A1), hereinafter "Matsumoto".

Regarding claim 2, the modification of AAPA with Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1, wherein the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)**.

The combination of AAPA and Uesugi does not disclose controlling read enable signals for controlling the data output stored in the slot buffer.

Matsumoto teaches the use of read enable signals for accessing data from a buffer which is activated when a determination is made that the buffer contains valid data, and is deactivated when it is determined the data in the buffer is invalid **(Para [0093])**. Matsumoto suggests that in order to meet increasing demands on channel capacities and for higher speed channels, and improved buffer access method is required **(Para [0007]-[0008])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the buffer access methods taught by Matsumoto in the device taught by AAPA as modified by Uesugi in order to access valid data stored in a buffer by using a read enable signal because the suggestion lies in Matsumoto that this can result in higher speed data transfers.

Regarding claim 13, AAPA in view of Uesugi disclose the demodulation method in the OFDMA based packet communication system of claim 121 [*sic*], wherein

the signals are stored in stage a) until the modulation methods for each sub-channels are analyzed **(AAPA: Fig. 2, Slot Buffers 26, it would be obvious that the symbols demapped as taught by Uesugi could be stored in the Slot buffer of Fig. 2)**; and demodulating the valid data **(AAPA: Para [10])**

Uesugi discloses the data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)**.

The combination of AAPA and Uesugi does not explicitly teach reading only valid data from among the signals are read by the modulation methods for each sub-channels analyzed in stage b).

Matsumoto teaches the use of read enable signals for accessing data from a buffer which is activated when a determination is made that the buffer contains valid data, and is deactivated when it is determined the data in the buffer is invalid **(Para [0093])**. Matsumoto suggests that in order to meet increasing demands on channel capacities and for higher speed channels, and improved buffer access method is required **(Para [0007]-[0008])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the buffer access methods taught by Matsumoto in the device taught by AAPA as modified by Uesugi in order to access the valid portion of the data acquired by the demapping process of Uesugi stored in a buffer by using a read enable signal because the suggestion lies in Matsumoto that this can result in higher speed data transfers.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Uesugi, furthering view of Lassen et al. (US 2002/0087685 A1), hereinafter "Lassen".

Regarding claim 3, AAPA in view of Uesugi discloses the demodulation apparatus in the OFDMA based packet communication system of claim 1 wherein the

data demapped (i.e. demodulated) using the maximum modulation ratio results in varying amounts of valid data **(Fig. 3, six significant bits S0-S5; Fig. 5, four significant bits, S0-S3; Fig. 7, two significant bits S0-S1)** but does not explicitly recite the limitation of claim 3.

Lassen teaches storing symbols in a temporary storage buffer **(Fig. 3, Decoder Temporary Storage Buffer 255)** prior to decoding. Lassen discloses the temporary storage can be faster access storage such as RAM in which the symbols are accessed from the RAM based on a schedule (i.e. valid data) **(Para [0241])**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use RAM as taught by Lassen because the suggestion lies in Lassen that RAM provides faster memory access.

Response to Arguments

6. Applicant's arguments filed 16 June 2010 have been fully considered but they are not persuasive.

7. Claims 1-11 stand as rejected under 35 U.S.C § 112 2nd paragraph as indefinite. Applicant has pointed to the description of paragraph [44] of the original disclosure as a description of the structure for "analyzing modulation methods for each of the sub-channels." It is the examiner's position that this paragraph provides functional language but does not provide a description of a structure for "analyzing modulation methods for each of the sub-channels." In fact, applicant's disclosure provides a figure **(Fig. 10)** depicting a box that performs a function and a description of the function performed by

the box. Such functional description does not advise one of ordinary skill in the art of the structure utilized to perform the analysis. As such, the examiner maintains the rejection of claims 1-11 under 35 U.S.C § 112 2nd paragraph.

8. With respect to arguments presented regarding the prior art rejections of claim 1, AAPA in the background of the invention describes an apparatus and method in which the MAP information related to a transmission must be analyzed by a channel decoder in order to determine the modulation method used in the transmission in order to perform the QAM demapping process to the data bursts **(Para [11], [13])**. In such a scenario, the data that is output from the QAM demapper would be valid data. Fig. 2 depicts slot buffers in which the data output form the QAM demapper is stored. As shown above, the data in the prior art slot buffers is valid data because the data has been decoded according to the modulation methods that were analyzed by the channel decoder. AAPA indicates a "[channel] is QAM demapped in a QAM (Quadrature Amplitude Modulation) demapper. It is then channel decoded in a channel decoder 27 through a slot buffer 26, and it is finally demodulated." Because the prior art demodulator described in AAPA performs QAM demapping based on the modulation methods analyzed by the channel decoder, resulting in valid data (or only valid data) output from the QAM demapper which is channel decoded through a slot buffer and finally demodulated, it is examiner's position that this substantially describes the claim limitation of "reading valid data from the data stored in the slot buffer, based on the analyzed modulation methods for each sub channels and demodulating the valid data, and outputting demodulated data."

The teachings of the art of record Uesugi et al. (US 2002/0114379 A1) disclose that OQPSK, 16QAM and 64QAM (among others) can be demapped utilizing a 64QAM constellation to allow for demapping received sub channels with a decrease in delay. Based on the teachings of Uesugi et al. and AAPA, it would have been obvious to one of ordinary skill in the art that one would still need to analyze the modulation methods of each sub-channel in order to know how many bits, of the 6 bits that result from the 64QAM demapping process, were relevant to the sub-channel being demodulated in order to coherently receive the information carried in the transmission (i.e. 2 for QPSK, 4 for 16QAM and 6 for 64QAM). Therefore, claim 1 is fairly suggested by the combination of AAPA and the teachings of Uesugi et al. Furthermore, the method of claim 12 is the method performed by the apparatus of claim 1, and is also rendered obvious by the combination of prior art applied to claim 1.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joey Bednash whose telephone number is (571)270-7500. The examiner can normally be reached on Mon-Fri 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joey Bednash/
Examiner, Art Unit 2461

/Huy D Vu/

Supervisory Patent Examiner, Art Unit 2461